Prateek Singh

Embedded / Firmware Engineer

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Education

University of Waterloo | B.A.Sc. in Mechatronics Engineering — Graduating Oct 2026

- Specialized courses: MTE 544 | ME 547 | ECE 488 | MTE 421 | MTE 420

Skills

Languages: C • Rust • C++ • Verilog • Python • Assembly • MATLAB • Java

Firmware: Bare-metal • embassy-stm32 async • DMA • interrupts • bootloaders

Protocols: CAN • I²C • SPI • UART • SAI / I²S • UDS (ISO 14229) • USB OTG

Hardware: STM32H755ZI • STM32F446RE • GW2A-LV18 • GW5A-LV25 • ESP32 • Arduino • Oscilloscope • Soldering

Tools: Gowin IDE • PSIM • defmt / RTT • GDB

Experience

Firmware Engineer | Co-op | Timberwolf Automotive — May 2026 – Aug 2026

- Developed safety-critical VCU/BMS firmware in Rust (embassy-stm32) on an STM32H7 for an EV powertrain — high-voltage precharge and contactor control with weld/interlock detection, isolation monitoring, and low-voltage supervision
- Designed the firmware's safety architecture — timestamped inter-task signals with staleness deadlines and typed fail-safes, a centralized prioritized fault manager, and a contention-free multi-ADC ownership model
- Built a classical CAN communication layer integrating multiple supplier ECUs

Mechanical Coordinator | Co-op | Toronto District School Board — May 2023 – Aug 2023

- Coordinated HVAC system documentation and mechanical drawings across multiple school facilities

Lab Assistant | Co-op | Jenike & Johanson Ltd. — Sept 2020 – Dec 2020

- Analyzed particle size distribution test data to inform bulk material handling design decisions

Projects

FPGA IR Night Vision Headset | MTE Capstone | Project page ↗ — Sept 2025 – Mar 2026

- Built a real-time IR video pipeline in Verilog on a Tang Primer 25K FPGA with OV5640 DVP capture (YUV422; 25 MHz DCLK, ~115 MHz PCLK) driving 2× FLCOS displays at 60 Hz, initialized with bit-bang I²C sequencer bringing up camera and panels
- Achieved pixel-to-pixel latency (45.6 ns – 549 µs) without a full frame buffer with IR camera pipeline

FPGA CNN Inference Accelerator | Tang Primer 20K | — May 2026 – July 2026

- Designed and implemented a 3-layer CNN (8/16/32 filter CONV layers, 3×3 kernels) accelerator in Verilog on a Tang Primer 20K FPGA to perform real-time finger count classification from a live camera feed within a 20,736-LUT / 828KB-BSRAM FPGA budget
- Built a real time video preprocessing pipeline from OV5640 camera (DVP/YUV422), luma extraction, nearest neighbor downsampling (640×480 → 96×96), int8 normalization

STM32 Quadcopter Firmware Drivers | Project page ↗ — Sept 2025 – Present

- Programmed bare-metal STM32F4 drivers for I2C, PWM, and USART
- Implemented I²C communication for configuration of the MPU6050 IMU and LIS3MDL magnetometer

Autonomous Mobile Robot Navigation System | MTE 544 | Project page ↗ — Sept 2025 – Dec 2025

- Implemented an A* path planner and a PID trajectory controller for autonomous robot navigation
- Built a particle-filter localization system using LiDAR and odometry data to estimate robot pose in real time

8-bit Breadboard Computer | 6502 Computer | VGA Card | Project page ↗ — Sept 2024 – Aug 2025

- Built an operating Turing complete 8-bit computer with integrated circuits on breadboards and a custom assembly language
- Programmed the computer with assembly and executed programs stored in a breadboard built EEPROM
- Constructed a 6502 computer with a discrete-logic VGA card generating real HSYNC/VSYNC signals at correct pixel clock frequencies